



2N7002

N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

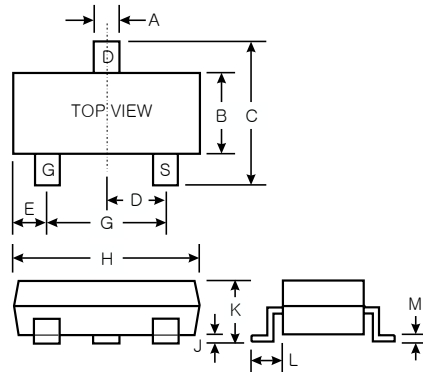
Voltage - 60 Volts Drain Current - 115 mAmps

FEATURES

- Low On-Resistance: $R_{DS(ON)}$
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- ESD Protected :1000V

MECHANICAL DATA

- Case: SOT-23, Molded Plastic
- Case Material - UL Flammability Rating Classification 94V-0
- Terminals: Solderable per MIL-STD-202, Method 208
- Marking: Device Code
- Weight: 0.008 grams (approx.)

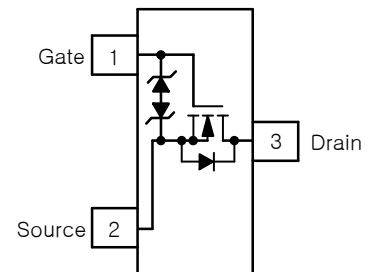


SOT-23		
Dim	Min	Max
A	0.37	0.51
B	1.19	1.40
C	2.10	2.50
D	0.89	1.05
E	0.45	0.61
G	1.78	2.05
H	2.65	3.05
J	0.013	0.15
K	0.89	1.10
L	0.45	0.61
M	0.076	0.178
All Dimensions in mm		

● MAXIMUM RATING ($T_a = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V _{dc}
Drain-Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$)	V_{DGR}	60	V _{dc}
Drain Current	I_D	± 115	mAdc
- Continuous $T_C = 25^\circ\text{C}$ (Note 1.)	I_D	± 75	
- Pulsed (Note 2.)	I_{DM}	± 800	
Gate-Source Voltage	V_{GS}	± 20	V _{dc}
- Continuous	V_{GS}	± 40	V _{pk}
- Non-repetitive ($t_p \leq 50\ \mu\text{s}$)			

Simplified Schematic



(Top View)

● THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 3.) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate, (Note 4.) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.
3. FR-5 = $1.0 \times 0.75 \times 0.062$ in.
4. Alumina = $0.4 \times 0.3 \times 0.025$ in 99.5% alumina.



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RATINGS AND CHARACTERISTIC CURVES

Switching Waveforms and Test Circuit

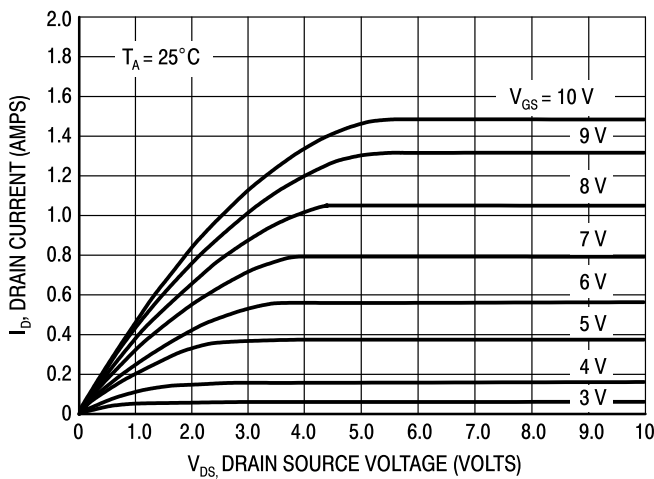
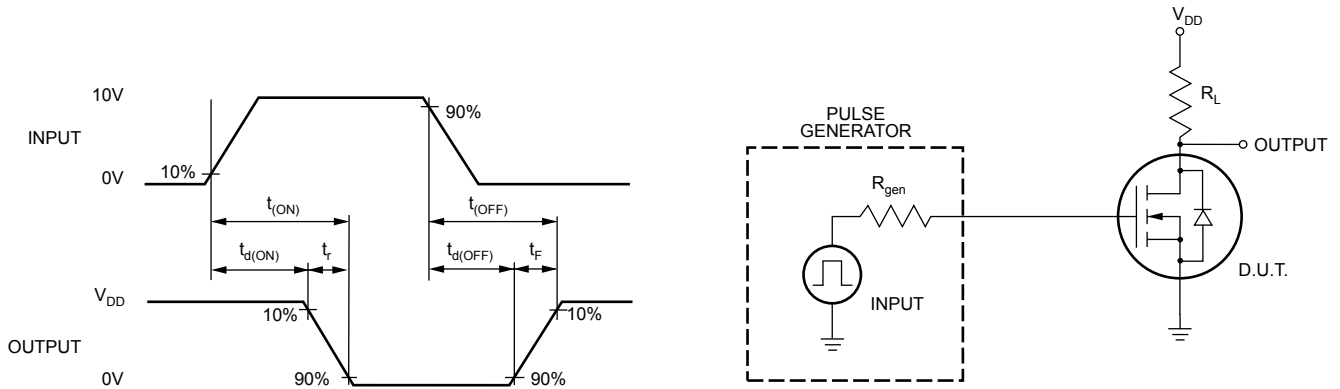


Figure 1. Ohmic Region

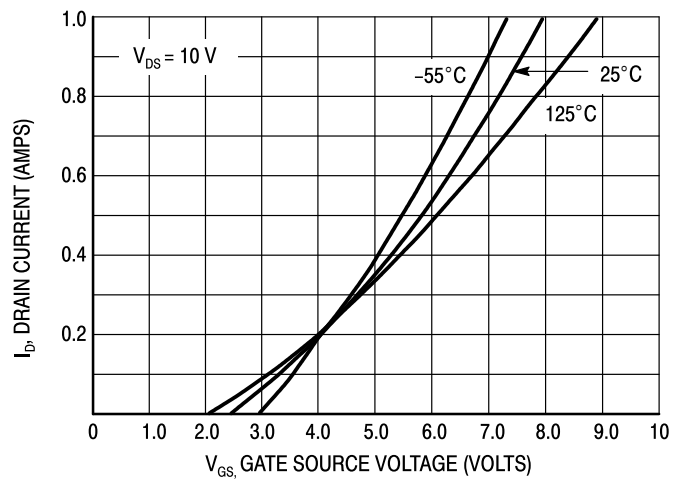


Figure 2. Transfer Characteristics

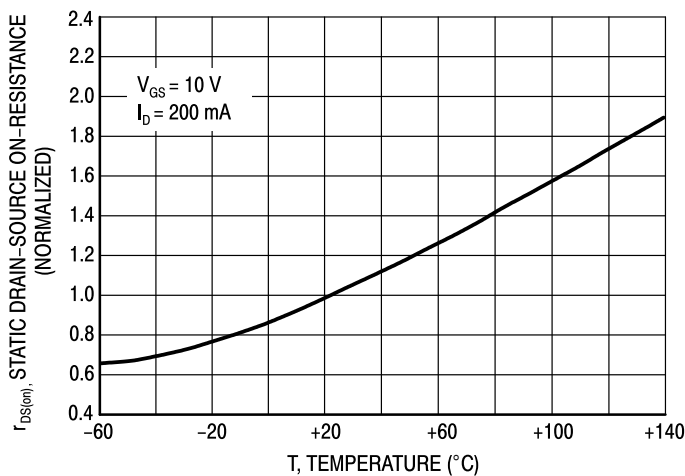


Figure 3. Temperature versus Static Drain-Source On-Resistance

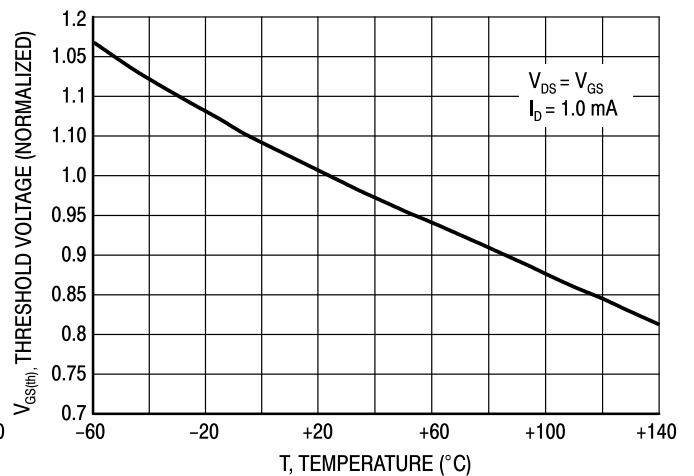


Figure 4. Temperature versus Gate Threshold Voltage